RDA5807FP

SINGLE-CHIP BROADCAST FM RADIO TUNER

Rev.1.2–April.2012

1 General Description

The RDA5807FP series is the newest generation single-chip broadcast FM stereo radio tuner with fully integrated synthesizer, IF selectivity, RDS/RBDS and MPX decoder. The tuner uses the CMOS process, support multi-interface and require the least external component. The package sizes is SOP16. It is completely adjustment-free. All these make it very suitable for portable devices.

The RDA5807FP series has a powerful low-IF digital audio processor, this make it have optimum sound quality with varying reception conditions.

The RDA5807FP series support frequency range is from 50MHz

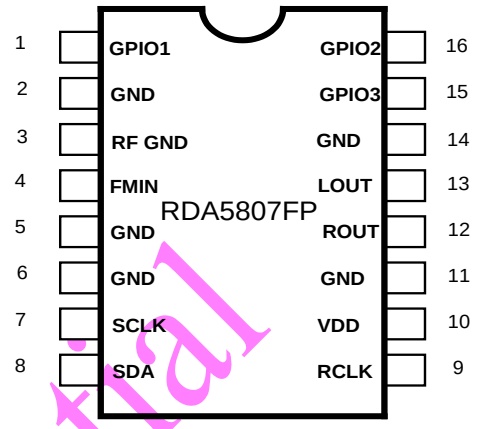


Figure1-1. RDA5807FP Top View

1.1 Features

- CMOS single-chip fully-integrated FM tuner
- Low power consumption
  - Total current consumption lower than 20mA at 3.0V power supply when under normal situation
- Support worldwide frequency band
  - 50 -108 MHz
- Support flexible channel spacing mode
  - 100KHz, 200KHz, 50KHz and 25KHz
- Support RDS/RBDS
- Digital low-IF tuner
  - Image-reject down-converter
  - High performance A/D converter
  - IF selectivity performed internally
- Fully integrated digital frequency synthesizer
  - Fully integrated on-chip RF and IF VCO
  - Fully integrated on-chip loop filter
- Autonomous search tuning
- Support 32.768KHz crystal oscillator
- Digital auto gain control (AGC)
- Digital adaptive noise cancellation
  - Mono/stereo switch
  - Soft mute
  - High cut
- Programmable de-emphasis (50/75 μs)
- Receive signal strength indicator (RSSI) and SNR
- Bass boost
- Volume control and mute
- I^2S digital output interface
- Line-level analog output voltage
- 32.768 KHz 12M,24M,13M,26M,19.2M,38.4MHz Reference clock
- Only support 2-wire bus interface
- Directly support 32Ω resistance loading
- Integrated LDO regulator
  - 2.7 to 3.3 V operation voltage
- SOP16 package.

1.2 Applications

- Cellular handsets
- MP3, MP4 players
- Portable radios
- PDAs, Notebook

2 Table of Contents

3 Functional Description

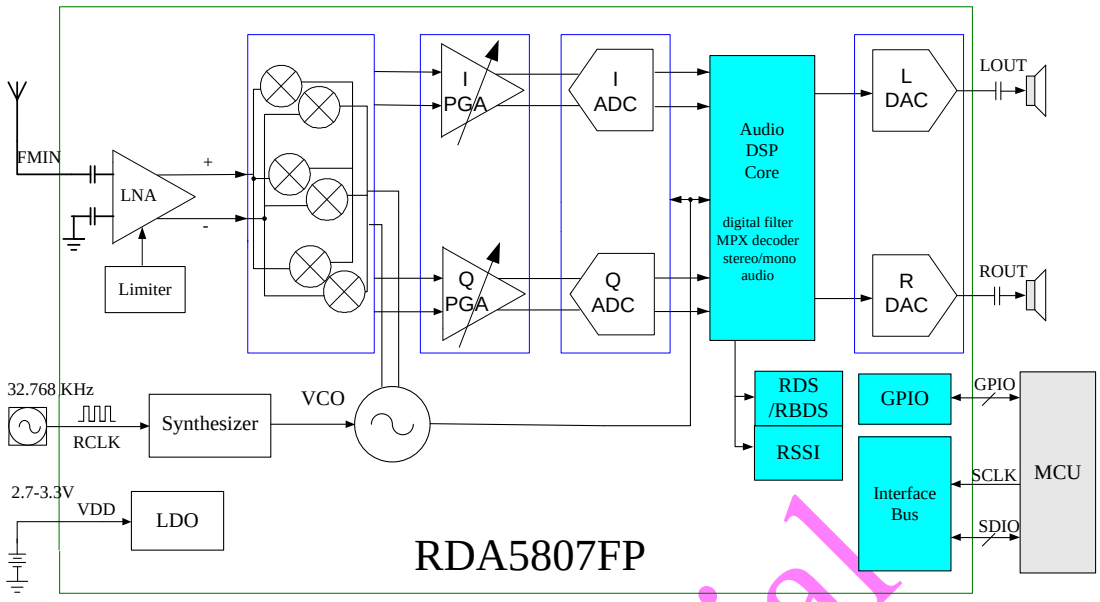


Figure 3-1. RDA5807FP FM Tuner Block Diagram

3.1 FM Receiver

The receiver uses a digital low-IF architecture that avoids the difficulties associated with direct conversion while delivering lower solution cost and reduces complexity, and integrates a low noise amplifier (LNA) supporting the FM broadcast band (50 to 115MHz), a multi-phase image-reject mixer array, a programmable gain control (PGA), a high resolution analog-to-digital converters (ADCs), an audio DSP and a high-fidelity digital-to-analog converters (DACs).

The limiter prevents overloading and limits the amount of intermodulation products created by strong adjacent channels.

The multi-phase mixer array down converts the LNA output differential RF signal to low-IF, it also has image-reject function and harmonic tones rejection.

The PGA amplifies the mixer output IF signal and then digitized with ADCs.

The DSP core finishes the channel selection, FM demodulation, stereo MPX decoder and output audio signal. The MPX decoder can autonomous switch from stereo to mono to limit the output noise.

The DACs convert digital audio signal to analog and change the volume at same time. The DACs has low-pass feature and -3dB frequency is about 30 KHz.

3.2 Synthesizer

The frequency synthesizer generates the local oscillator signal which divide to multi-phase, then be used to downconvert the RF input to a constant low intermediate frequency (IF). The synthesizer reference clock is 32.768 KHz.

The synthesizer frequency is defined by bits CHAN[9:0] with the range from 50MHz to 115MHz.

3.3 Power Supply

The RDA5807FP integrated one LDO which supplies power to the chip. The external supply voltage range is 2.7-3.3 V.

3.4 RESET and Control Interface select

The RDA5807FP is RESET itself When VDD is Power up. And also support soft reset by trigger 02H BIT1 from 0 to 1. The RDA5807FP only support I^2C control interface bus mode.

3.5 Control Interface

The RDA5807FP only supports I^2C control interface.

The I^2C interface is compliant to I^2C Bus Specification 2.1. It includes two pins: SCLK and SDIO. A I^2C interface transfer begins with START condition, a command byte and data bytes, each byte has a followed ACK (or NACK) bit, and ends with STOP condition. The command byte includes a 7-bit chip address (0010000b) and a R/W bit. The ACK (or NACK) is always sent out by receiver. When in write transfer, data bytes is written out from MCU, and when in read transfer, data bytes is read out from RDA5807FP. There is no visible register address in I^2C interface transfers. The I^2C interface has a fixed start register address (0x02h for write transfer and 0x0Ah for read transfer), and an internal incremental address counter. If register address meets the end of register file, 0x3Ah, register address will wrap back to 0x00h. For write transfer, MCU programs registers from register 0x02h high byte, then register 0x02h low byte, then register 0x03h high byte, till the last register. RDA5807FP always gives out ACK after every byte, and MCU gives out STOP condition when register programming is finished. For read transfer, after command byte from MCU, RDA5807FP sends out register 0x0Ah high byte, then register 0x0Ah low byte, then register 0x0Bh high byte, till receives NACK from MCU. MCU gives out ACK for data bytes besides last data byte. MCU gives out NACK for last data byte, and then RDA5807FP will return the bus to MCU, and MCU will give out STOP condition.

3.6 I^2S Audio Data Interface

The RDA5807FP supports I^2S (Inter_IC Sound Bus) audio interface. The interface is fully compliant with I^2S bus specification. When setting I2SEN bit high, RDA5807FP will output SCK, WS, SD signals from GPIO3, GPIO1, GPIO2 as I^2S master and transmitter, the sample rate is 48Kbps，44.1kbps,32kbps….. RDA5807FP also support as I^2S slaver mode and transmitter, the sample rate is less than 100kbps.

3.7 GPIO Outputs

The RDA5807FP has three GPIOs. The function of GPIOs could programmed with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0] and I2SEN.

If I2SEN is set to low, GPIO pins could be programmed to output low or high or high-Z, or be programmed to output interrupt and stereo indicator with bits GPIO1[1:0], GPIO2[1:0], GPIO3[1:0]. GPIO2 could be programmed to output a low interrupt (interrupt will be generated only with interrupt enable bit STCIEN is set to high) when seek/tune process completes. GPIO3 could be programmed to output stereo indicator bit ST.

Constant low, high or high-Z functionality is available regardless of the state of VDD supplies or the ENABLE bit.

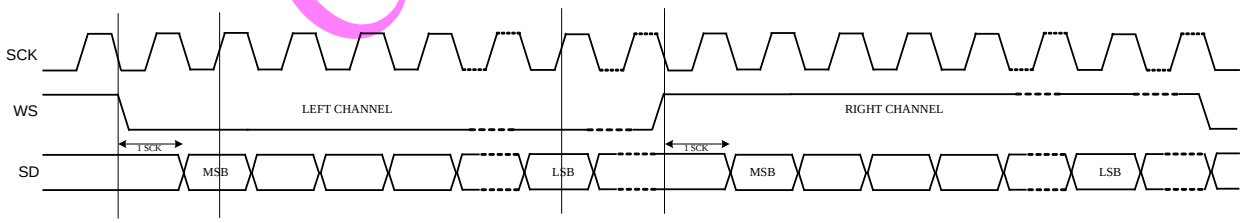


Figure 3-2 I2S Digital Audio Format

4 Electrical Characteristics

Table 4-1 DC Electrical Specification (Recommended Operation Conditions):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
VDD	Supply Voltage	2.7	3.0	3.3	V
T_{amb}	Ambient Temperature	-20	27	+75	℃
V_{IL}	CMOS Low Level Input Voltage	0		0.3*VDD	V
V_{IH}	CMOS High Level Input Voltage	0.7*VDD		VDD	V
V_{TH}	CMOS Threshold Voltage		0.5*VDD		V

Table 4-2 DC Electrical Specification (Absolute Maximum Ratings):

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNIT
T_{amb}	Ambient Temperature	-40		+90	°C
I_{IN}	Input Current (1)	-10		+10	mA
V_{IN}	Input Voltage(1)	-0.3		VDD+0.3	V
V_{lna}	LNA FM Input Level			+10	dBm

Notes:

1. For Pin: SCLK, SDIO

Table 4-3 Power Consumption Specification

(VDD = 3.0V, T_A = 25℃, unless otherwise specified)

SYMBOL	DESCRIPTION	CONDITION	TYP	UNIT
I_{VDD}	Supply Current(1)	ENABLE=1	20	mA
I_{VDD}	Supply Current(2)	ENABLE=1	21	mA
I_{PD}	Powerdown Current	ENABLE=0	25	μA

Notes:

1. **For strong input signal condition**
2. **For weak input signal condition**

5 Receiver Characteristics

Table 5-1 Receiver Characteristics

(VDD = 3 V, T_A = 25 °C, unless otherwise specified)

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNIT
General specifications							
F_{in}	FM Input Frequency Range	Adjust BAND Register		50		115	MHz
V_{rf}	Sensitivity[1,2,3]	S/N=26dB	50MHz	-	1.4	1.8	μV EMF
			65MHz	-	1.2	1.5	
			88MHz	-	1.2	1.5	
			98MHz	-	1.3	1.5	
			108MHz	-	1.3	1.5	
			115MHz	-	1.3	1.8	
$IP3_{in}$	Input IP3[4]	AGCD=1		80	-	-	dBμV
α_{am}	AM Suppression[1,2]	m=0.3		60	-	-	dB
S_{200}	Adjacent Channel Selectivity	±200KHz		50	70	-	dB
S_{400}	400KHz Selectivity	±400KHz		60	85	-	dB
V_{AFL}; V_{AFR}	Audio L/R Output Voltage[1,2] (Pins LOUT and ROUT)	Volume [3:0] =1111		-	360	-	mV
S/N	Maximum Signal to Noise Ratio[1,2,3,5]		Mono[2]	55	57	-	dB
			Stereo[6]	53	55	-	
α_{SCS}	Stereo Channel Separation			35	-	-	dB
R_L	Audio Output Loading Resistance	Single-ended		32	-	-	Ω
THD	Audio Total Harmonic Distortion[1,3,6]	Volume[3:0] =1111	R_{load}=1KΩ	-	0.15	0.2	%
			R_{load}=32Ω	-	0.2	-	
α_{AOI}	Audio Output L/R Imbalance[1,6]			-	-	0.05	dB
R_{mute}	Mute Attenuation Ratio[1]	Volume[3:0]=0000		60	-	-	dB
BW_{audio}	Audio Response[1]	1KHz=0dB	Low Freq[9]	-	100	-	Hz
		±3dB point	High Freq	-	14	-	
Pins FMIN, LOUT, ROUT							
V_{com_rfin}	Pins FMIN Input Common Mode Voltage				**0**		V
V_{com}	Audio Output Common Mode Voltage[8]			1.0	1.05	1.1	V

Notes: 1. F_{in}=65 to 115MHz; F_{mod}=1KHz; de-emphasis=75μs; MONO=1; L=R unless noted otherwise;

2. Δf=22.5KHz; 3. B_{AF} = 300Hz to 15KHz, RBW <=10Hz; 4. $|f_2-f_1|>1$MHz, $f_0=2xf_1-f_2$, AGC disable, F_{in}=76 to 108MHz;
5. P_{RF}=60dB$_U$V; 6. Δf=75KHz,fpilot=10% 7. Measured at V_{EMF} = 1 m V, f_{RF} = 65 to 108MHz
8. At LOUT and ROUT pins 9. Adjustable

6 Serial Interface

6.1 I²C Interface Timing

Table 6-1 I²C Interface Timing Characteristics

(VDD = 3.0 V, T_A = 25°C, unless otherwise specified)

PARAMETER	SYMBOL	TEST CONDITION	MIN	TYP	MAX	UNIT
SCLK Frequency	f_{scl}		0	-	400	KHz
SCLK High Time	t_{high}		0.6	-	-	µs
SCLK Low Time	t_{low}		1.3	-	-	µs
Setup Time for START Condition	$t_{su:sta}$		0.6	-	-	µs
Hold Time for START Condition	$t_{hd:sta}$		0.6	-	-	µs
Setup Time for STOP Condition	$t_{su:sto}$		0.6	-	-	µs
SDIO Input to SCLK↑ Setup	$t_{su:dat}$		100	-	-	ns
SDIO Input to SCLK↓ Hold	$t_{hd:dat}$		0	-	900	ns
STOP to START Time	t_{buf}		1.3	-	-	µs
SDIO Output Fall Time	$t_{f:out}$		20+0.1C_b	-	250	ns
SDIO Input, SCLK Rise/Fall Time	$t_{r:in}$ / $t_{f:in}$		20+0.1C_b	-	300	ns
Input Spike Suppression	t_{sp}		-	-	50	ns
SCLK, SDIO Capacitive Loading	C_b		-	-	50	pF
Digital Input Pin Capacitance					5	pF

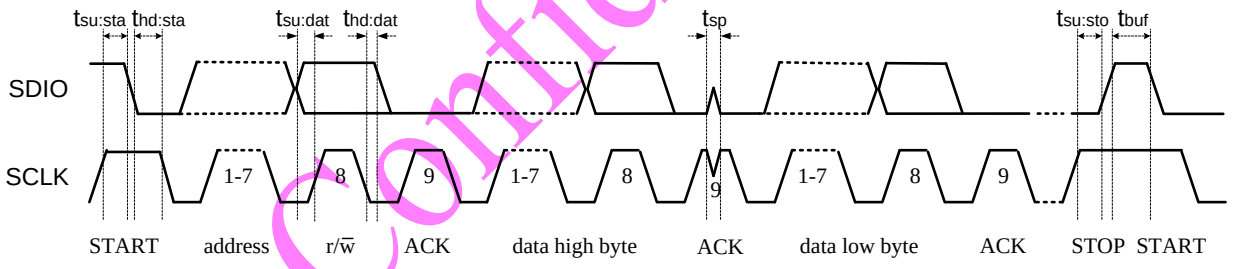


Figure 6-1. I²C Interface Write Timing Diagram

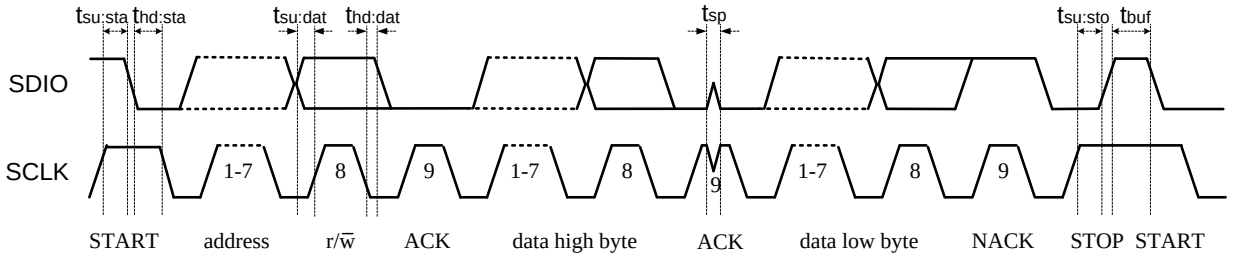


Figure 6-2. I²C Interface Read Timing Diagram

7 Register Definition

REG	BITS	NAME	FUNCTION	DEFAULT
00H	15:8	CHIPID[7:0]	Chip ID.	0x58
02H	15	DHIZ	Audio Output High-Z Disable. *0 = High impedance; 1 = Normal operation*	0
	14	DMUTE	Mute Disable. *0 = Mute; 1 = Normal operation*	0
	13	MONO	Mono Select. *0 = Stereo; 1 = Force mono*	0
	12	BASS	Bass Boost. *0 = Disabled; 1 = Bass boost enabled*	0
	11	RCLK NON-CALIBRATE MODE	0=RCLK clock is always supply 1=RCLK clock is not always supply when FM work (when 1, RDA5807FP can't directly support -20℃~70℃ temperature. Only suppory ±20℃ temperature swing from tune point)	0
	10	RCLK DIRECT INPUT MODE	1=RCLK clock use the directly input mode	0
	9	SEEKUP	Seek Up. *0 = Seek down; 1 = Seek up*	0
	8	SEEK	Seek. *0 = Disable stop seek; 1 = Enable* *Seek begins in the direction specified by* SEEKUP *and ends when a channel is found, or the entire band has been searched.* *The* SEEK *bit is set low and the* STC *bit is set high when the seek operation completes.*	0
	7	SKMODE	Seek Mode 0 = wrap at the upper or lower band limit and continue seeking 1 = stop seeking at the upper or lower band limit	0
	6:4	CLK_MODE[2:0]	000=32.768kHz 001=12Mhz 101=24Mhz 010=13Mhz 110=26Mhz 011=19.2Mhz 111=38.4Mhz	000
	3	RDS_EN	RDS/RBDS enable If 1, rds/rbds enable	0
	2	NEW_METHOD	New Demodulate Method Enable, can improve the receive sensitivity about 1dB.	0
	1	SOFT_RESET	Soft reset. If 0, not reset; If 1, reset.	0

REG	BITS	NAME	FUNCTION	DEFAULT
	0	**ENABLE**	**Power Up Enable.** ***0 = Disabled; 1 = Enabled***	0
03H	**15:6**	**CHAN[9:0]**	**Channel Select.** **BAND =** ***0*** ***Frequency =*** ***Channel Spacing (kHz) x* CHAN+ *87.0 MHz*** **BAND =** ***1or 2*** ***Frequency =*** ***Channel Spacing (kHz) x* CHAN + *76.0 MHz*** **BAND =** ***3*** ***Frequency =*** ***Channel Spacing (kHz) x* CHAN + *65.0 MHz*** **CHAN** ***is updated after a seek operation.***	0x00
	5	**DIRECT MODE**	**Directly Control Mode, Only used when test.**	0
	4	**TUNE**	**Tune** **0 = Disable** **1 = Enable** **The tune operation begins when the TUNE bit is set high. The STC bit is set high when the tune operation completes.** **The tune bit is reset to low automatically when the tune operation completes..**	0
	3:2	**BAND[1:0]**	**Band Select.** **00 = 87–108 MHz (US/Europe)** **01 = 76–91 MHz (Japan)** **10 = 76–108 MHz (world wide)** **11[1] = 65 –76 MHz （East Europe） or 50-65MHz**	00
	1:0	**SPACE[1:0]**	**Channel Spacing.** **00 = 100 kHz** **01 = 200 kHz** **10 = 50kHz** **11 = 25KHz**	00
04H	**15**	**RSVD**	**Reserved**	0
	14	**STCIEN**	**Seek/Tune Complete Interrupt Enable.** **0 = Disable Interrupt** **1 = Enable Interrupt** **Setting STCIEN = 1 will generate a low pulse on GPIO2 when the interrupt occurs.**	0
	13:12	**RSVD**	**Reserved**	00
	11	**DE**	**De-emphasis.** ***0 = 75 μs; 1 = 50 μs***	0
	10	**RSVD**	**Reserved**	
	9	**SOFTMUTE_EN**	**If 1, softmute enable**	1
	8	**AFCD**	**AFC disable.** **If 0, afc work;**	0

[1] If 0x07h_bit<9> (band)=1, 65-76MHz; =0, 50-76MHz

REG	BITS	NAME	FUNCTION	DEFAULT
			If 1, afc disabled.	
	7	**RSVD**	**Reserved**	
	6	**I2S_ENABLED**	**I2S bus enable** **If 0, disabled;** **If 1, enabled.**	0
	5:4	**GPIO3[1:0]**	**General Purpose I/O 3.** ***00 = High impedance*** ***01 = Mono/Stereo indicator (ST)*** ***10 = Low*** ***11 = High***	00
	3:2	**GPIO2[1:0]**	**General Purpose I/O 2.** ***00 = High impedance*** ***01 = Interrupt (INT)*** ***10 = Low*** ***11 = High***	00
	1:0	**GPIO1[1:0]**	**General Purpose I/O 1.** ***00 = High impedance*** ***01 = Reserved*** ***10 = Low*** ***11 = High***	00
05H	**15**	**INT _MODE**	**If 0, generate 5ms interrupt;** **If 1, interrupt last until read reg0CH action occurs.**	1
	14:12	**RSVD**	**Reserved**	000
	11:8	**SEEKTH[3:0][2]**	**Seek SNR threshold value**	1000
	7:6	**LNA_PORT_SEL[1:0]**	**LNA input port selection bit:** **10: FMIN**	10
	5:4	**RSVD**	**Resvered**	00
	3:0	**VOLUME[3:0]**	**DAC Gain Control Bits (Volume).** **0000=min; 1111=max** **Volume scale is logarithmic** **When 0000, output mute and output impedance is very large**	1111
06H	**15**	**RSVD**	**reserved**	0
	14:13	**OPEN_MODE[1:0]**	**Open reserved register mode.** **11=open behind registers writing function** **others: only open behind registers reading function**	00
	12	**I2S_MODE[3]**	**If 0, master mode;** **If 1, slave mode.**	**0**
	11	**SW_LR[3]**	**Ws relation to l/r channel.** **If 0, ws=0 ->r, ws=1 ->l;** **If 1, ws=0 ->l, ws=1 ->r.**	**10**
	10	**SCLK_I_EDGE[3]**	**When I2S enable** **If 0, use normal sclk internally;**	**0**

[2] This value is SNR threshold for seeking, and the default value 1000 is about 32dB SNR.
3 This function is open when I2S_Enabled=1.

REG	BITS	NAME	FUNCTION	DEFAULT
			If 1, inverte sclk internally.	
	9	DATA_SIGNED[3]	If 0, I2S output unsigned 16-bit audio data. If 1, I2S output signed 16-bit audio data.	0
	8	WS_I_EDGE[3]	If 0, use normal ws internally; If 1, inverte ws internally.	0
	7:4	I2S_SW_CNT[4:0][3] Only valid in master mode	4'b1000: WS_STEP_48; 4'b0111: WS_STEP=44.1kbps; 4'b0110: WS_STEP=32kbps; 4'b0101: WS_STEP=24kbps; 4'b0100: WS_STEP=22.05kbps; 4'b0011: WS_STEP=16kbps; 4'b0010: WS_STEP=12kbps; 4'b0001: WS_STEP=11.025kbps; 4'b0000: WS_STEP=8kbps;	0000
	3	SW_O_EDGE[3]	If 1, invert ws output when as master.	0
	2	SCLK_O_EDGE[3]	If 1, invert sclk output when as master.	0
	1	L_DELY[3]	If 1, L channel data delay 1T.	0
	0	R_DELY[3]	If 1, R channel data delay 1T.	0
07H	15	RSVD	Reserved	0
	14:10	TH_SOFRBLEND[5:0]	Threshold for noise soft blend setting, unit 2dB	10000
	9	65M_50M MODE	Valid when band[1:0] = 2'b11 (0x03H_bit<3:2>) 1 = 65~76 MHz; 0 = 50~76 MHz.	1
	8	RSVD	Reserved	0
	7:2	SEEK_TH_OLD[4]	Seek threshold for old seek mode, Valid when Seek_Mode=001	000000
	1	SOFTBLEND_EN	If 1, Softblend enable	1
	0	FREQ_MODE	If 1, then freq setting changed. Freq = 76000(or 87000) kHz + freq_direct (08H) kHz.	0
0AH	15	RDSR	RDS ready 0 = No RDS/RBDS group ready(default) 1 = New RDS/RBDS group ready	0
	14	STC	Seek/Tune Complete. 0 = Not complete 1 = Complete The seek/tune complete flag is set when the seek or tune operation completes.	0
	13	SF	Seek Fail. *0 = Seek successful; 1 = Seek failure* *The seek fail flag is set when the seek operation fails to find a channel with an* RSSI *level greater than* SEEKTH[5:0].	0
	12	RDSS	RDS Synchronization 0 = RDS decoder not synchronized(default)	0

[4] 0x20H_bit<14:12>, Seek_Mode register. Default value is 000; When = 001, will add the 5807SP seek mode.

REG	BITS	NAME	FUNCTION	DEFAULT
			1 = RDS decoder synchronized **Available only in RDS Verbose mode**	
	11	**BLK_E**	**When RDS enable:** **1 = Block E has been found** **0 = no Block E has been found**	**0**
	10	**ST**	**Stereo Indicator.** ***0 = Mono; 1 = Stereo*** ***Stereo indication is available on* GPIO3 *by setting* GPIO3[1:0] =*01.***	1
	9:0	**READCHAN[9:0]**	**Read Channel.** **BAND = 0** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 87.0 MHz** **BAND = 1 or 2** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 76.0 MHz** **BAND = 3** **Frequency = Channel Spacing (kHz) x READCHAN[9:0]+ 65.0 MHz** **READCHAN[9:0] is updated after a tune or seek operation.**	8'h00
0BH	**15:9**	**RSSI[6:0]**	**RSSI.** **000000 = min** **111111 = max** **RSSI scale is logarithmic.**	0
	8	**FM TRUE**	**1 = the current channel is a station** **0 = the current channel is not a station**	0
	7	**FM_READY**	**1=ready** **0=not ready**	0
	<6:5>	**reserved**		0
	<4>	**ABCD_E**	**1= the block id of register 0cH,0dH,0eH,0fH is E** **0= the block id of register 0cH, 0dH, 0eH,0fH is A, B, C, D**	
	<3:2>	**BLERA[1:0]**	**Block Errors Level of RDS_DATA_0, and is always read as Errors Level of RDS BLOCK A (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)** **00= 0 errors requiring correction** **01= 1~2 errors requiring correction** **10= 3~5 errors requiring correction** **11= 6+ errors or error in checkword, correction not possible.** **Available only in RDS Verbose mode**	
	<1:0>	**BLERB[1:0]**	**Block Errors Level of RDS_DATA_1, and is always read as Errors Level of RDS BLOCK B (in RDS mode) or E (in RBDS mode when**	

REG	BITS	NAME	FUNCTION	DEFAULT
			ABCD_E flag is 1). **00= 0 errors requiring correction** **01= 1~2 errors requiring correction** **10= 3~5 errors requiring correction** **11= 6+ errors or error in checkword, correction not possible.** **Available only in RDS Verbose mode**	
0CH	**<15:0>**	**RDSA[15:0]**	**BLOCK A (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)**	16'h5803
0DH	**<15:0>**	**RDSB[15:0]**	**BLOCK B (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)**	16'h5804
0EH	**<15:0>**	**RDSC[15:0]**	**BLOCK C (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)**	16'h5808
0FH	**<15:0>**	**RDSD[15:0]**	**BLOCK D (in RDS mode) or BLOCK E (in RBDS mode when ABCD_E flag is 1)**	16'h5804

8 Pins Description

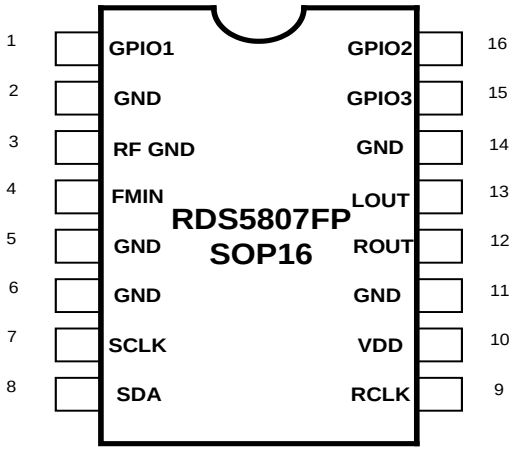
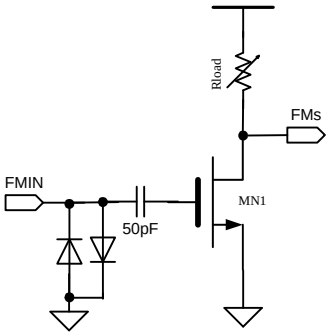
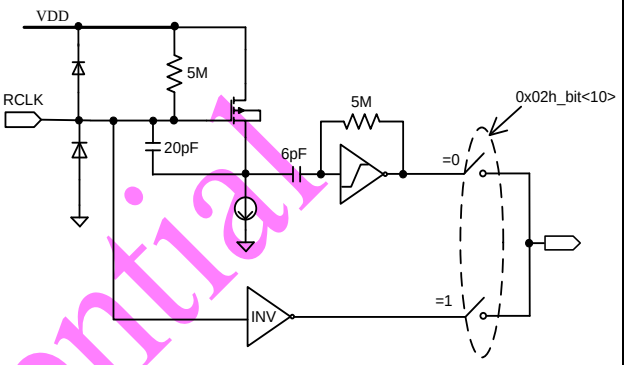
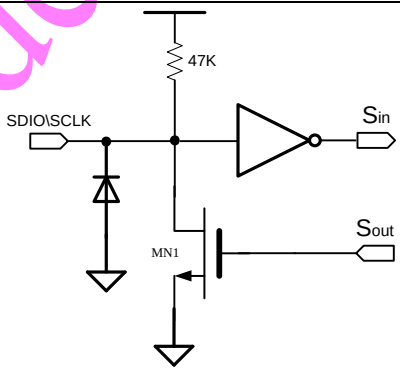
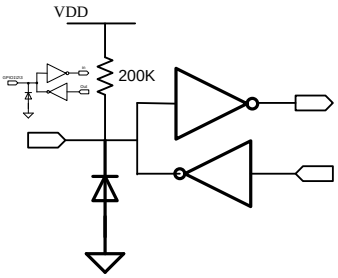


Figure 8-1. RDA5807FP Top View

Table 8-1 RDA5807FP SOP16 Pins Description

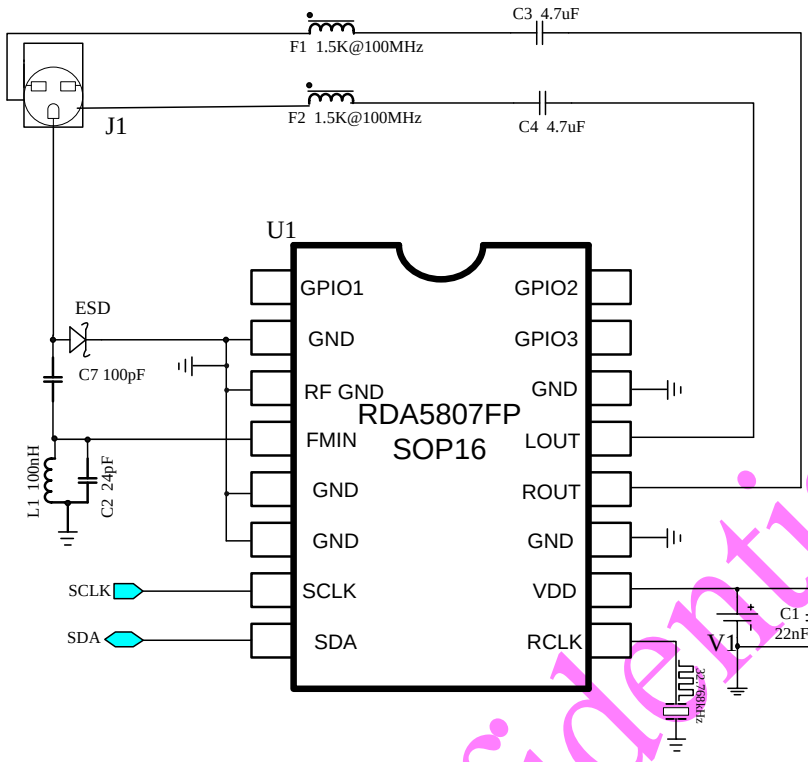
SYMBOL	PIN	DESCRIPTION
GND	2, 5,6,11,14	Ground. Connect to ground plane on PCB
RF GND	3	RF Ground. Connect to RF ground plane to PCB
FMIN	4	FM single input
RCLK	9	32.768KHz reference clock input
VDD	10	Power supply
LOUT,ROUT	13,12	Right/Left audio output
SCLK	7	Clock input for serial control bus
SDA	8	Data input/output for serial control bus
GPIO1,GPIO2,GPIO3	1,16,15	General purpose input/output

Table 8-2 Internal Pin Configuration

SYMBOL	PIN	DESCRIPTION
FMIN	4	
RCLK	9	
SCLK/SDIO	7/8	
GPIO1/GPIO2/GPIO3	1/16/15	

9 Application Diagram

9.1 RDA5807FP Common Application :



Notes:

1. J1: Common 32Ω Resistance Headphone;
2. V1: Power Supply (2.7~3.3V);
3. FM Choke (L1 and C2) for Audio Common and LNA Input Common;
4. Place C1 Close to 5807NP pin10.

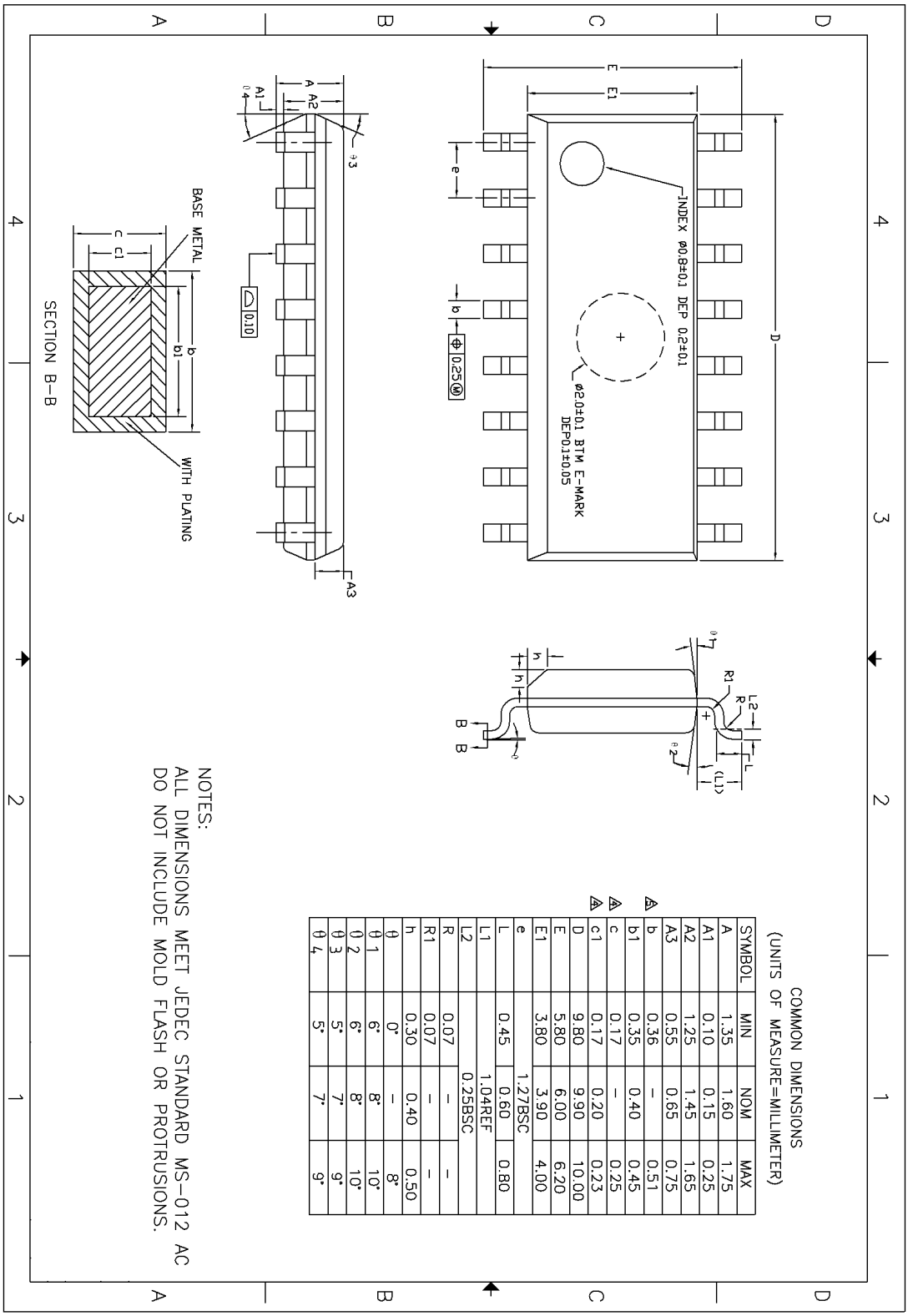
Figure 9-1. RDA5807FP FM Tuner Application Diagram (TCXO Application)

9.1.1 Bill of Materials:

COMPONENT	VALUE	DESCRIPTION	SUPPLIER
U1	RDA5807FP SOP16	Broadcast FM Radio Tuner	RDA
J1		Common 32Ω Resistance Headphone	
L1/C2	100nH/24pF	LC Chock for FMIN Input	Murata
C4,C5	125μF	Audio AC Couple Capacitors	Murata
C1	22nF	Power Supply Bypass Capacitor	Murata
C7	100pF	AC Couple Capacitors	Murata
ESD		TVS	
F1/F2	1.5K@100MHz	FM Band Ferrite	Murata

10 Physical Dimension

Figure 10-1 illustrates the package details for the RDA5807FP. The package is lead-free and RoHS-compliant.



COMMON DIMENSIONS
(UNITS OF MEASURE=MILLIMETER)

SYMBOL	MIN	NOM	MAX
A	1.35	1.60	1.75
A1	0.10	0.15	0.25
A2	1.25	1.45	1.65
A3	0.55	0.65	0.75
b	0.36	–	0.51
b1	0.35	0.40	0.45
c	0.17	–	0.25
c1	0.17	0.20	0.23
D	9.80	9.90	10.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27BSC	
L	0.45	0.60	0.80
L1		1.04REF	
L2		0.25BSC	
R	0.07	–	–
R1	0.07	–	–
h	0.30	0.40	0.50
θ	0°	–	8°
θ1	6°	8°	10°
θ2	6°	8°	10°
θ3	5°	7°	9°
θ4	5°	7°	9°

Figure 10-1. 16 PIN SOP PCB Land Pattern

11 PCB Land Pattern：

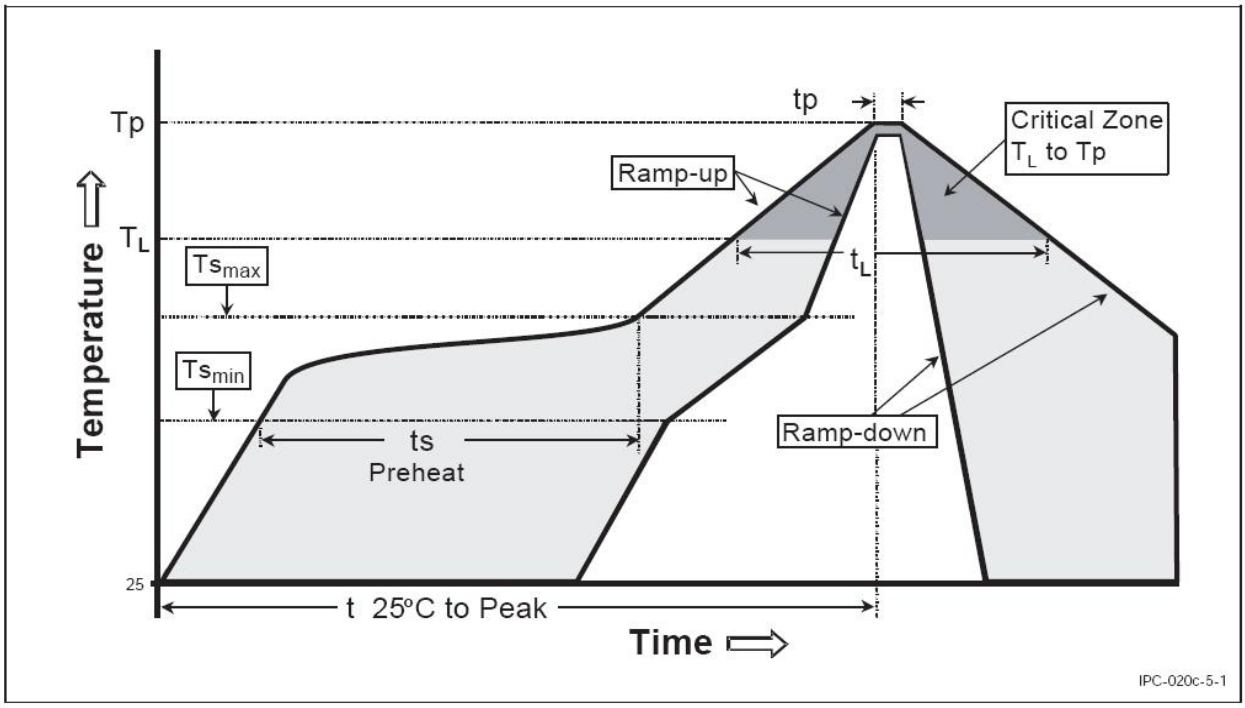


Figure 11.Classification Reflow Profile

Profile Feature	Sn-Pb Eutectic Assembly	Pb-Free Assembly
Average Ramp-Up Rate (T_{Smax} to T_p)	3 °C/second max.	3 °C/second max.
Preheat -Temperature Min (T_{smin}) -Temperature Max (T_{smax}) -Time (t_{smin} to t_{smax})	 100 °C 100 °C 60-120 seconds	 150 °C 200 °C 60-180 seconds
Time maintained above: -Temperature (T_L) -Time (t_L)	 183 °C 60-150seconds	 217°C 60-150 seconds
Peak /Classification Temperature(T_p)	See Table-II	See Table-III
Time within 5 °C of actual Peak Temperature (t_p)	10-30 seconds	20-40 seconds
Ramp-Down Rate	6 °C/second max.	6 °C/seconds max.
Time 25 °C to Peak	6 minutes max.	8 minutes max.

Temperature		

Table-I Classification Reflow Profiles

Package Thickness	**Volume mm^3 <350**	**Volume mm^3 ⩾350**
＜2.5mm	240 + 0/-5 °C	225 + 0/-5 °C
⩾2.5mm	225 + 0/-5 °C	225 + 0/-5 °C

Table – II SnPb Eutectic Process – Package Peak Reflow Temperatures

Package Thickness	**Volume mm^3 ＜350**	**Volume mm^3 350-2000**	**Volume mm^3 ＞2000**
＜1.6mm	260 + 0 °C *	260 + 0 °C *	260 + 0 °C *
1.6mm – 2.5mm	260 + 0 °C *	250 + 0 °C *	245 + 0 °C *
⩾2.5mm	250 + 0 °C *	245 + 0 °C *	245 + 0 °C *
*Tolerance : The device manufacturer/supplier **shall** assure process compatibility up to and including the stated classification temperature(this mean Peak reflow temperature + 0 °C. For example 260+ 0 °C) at the rated MSL Level.			

Table – III Pb-free Process – Package Classification Reflow Temperatures

Note 1: All temperature refer topside of the package. Measured on the package body surface.

Note 2: The profiling tolerance is + 0 °C, - X °C (based on machine variation capability)whatever

is required to control the profile process but at no time will it exceed - 5 °C. The producer assures process compatibility at the peak reflow profile temperatures defined in Table –III.

Note 3: Package volume excludes external terminals(balls, bumps, lands, leads) and/or non integral heat sinks.

Note 4: The maximum component temperature reached during reflow depends on package the thickness and volume. The use of convection reflow processes reduces the thermal gradients between packages. However, thermal gradients due to differences in thermal mass of SMD package may sill exist.

Note 5: Components intended for use in a “lead-free” assembly process **shall** be evaluated using the “lead free” classification temperatures and profiles defined in Table-I II III whether or not lead free.

RoHS Compliant

The product does not contain lead, mercury, cadmium, hexavalent chromium, polybrominated biphenyls (PBB) or polybrominated diphenyl ethers (PBDE), and are therefore considered RoHS compliant.

ESD Sensitivity

Integrated circuits are ESD sensitive and can be damaged by static electricity. Proper ESD techniques should be used when handling these devices.

12 Change List

REV	DATE	AUTHER	CHANGE DESCRIPTION
V1.0	2011-07-18	Chun Zhao, Yanan Liu	Original Draft.

Contact Information

RDA Microelectronics (Shanghai), Inc.
Suite 1108 Block A, e-Wing Center, 113 Zhichun Road Haidian District, Beijing
Tel: 86-10-62635360
Fax: 86-10-82612663
Postal Code: 100086

Suite 302 Building 2, 690 Bibo Road Pudong District, Shanghai
Tel: 86-21-50271108
Fax: 86-21-50271099
Postal Code: 201203